ABSTRACT OF THE DISCLOSURE

A circuit is provided which is constituted by TFTs of one conductivity type, and which is capable of outputting signals of a normal amplitude. When an input clock signal CK1 becomes a high level, each of TFTs (101, 103) is turned on to settle at a low level the potential at a signal output section (Out). A pulse is then input to a signal input section (In) and becomes high level. The gate potential of TFT (102) is increased to (VDD - V thN) and the gate is floated. TFT (102) is thus turned on. Then CK1 becomes low level and each of TFTs (101, 103) is turned off. Simultaneously, CK3 becomes high level and the potential at the signal output section is increased. Simultaneously, the potential at the gate of TFT (102) is increased to a level equal to or higher than (VDD + V thN) by the function of capacitor (104), so that the high level appearing at the signal output section (Out) becomes equal to VDD. When SP becomes low level; CK3 becomes low level; and CK1 becomes high level, the potential at the signal output section (Out) becomes low level again.